FORM PTO-1390 (Modified) (REV 11-2000) ♦ U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER	
211329US2PCT	
U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR	
09/926067	

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/DE00/00276	1 February 2000	26 February 1999

TITLE OF INVENTION

OPTIMIZED BUS CONNECTION FOR MANAGING BUS TRANSACTIONS

APPLICANT(S) FOR DO/EO/US

STOESS Annie et al.

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (24) indicated below.
4. ☒ The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c) (2))
   a. ☐ is attached hereto (required only if not communicated by the International Bureau).
   b. ☒ has been communicated by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☒ is attached hereto.
   b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))
   a. ☐ are attached hereto (required only if not communicated by the International Bureau).
   b. ☐ have been communicated by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).
10. ☐ An English language translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).
11. ☐ A copy of the International Preliminary Examination Report (PCT/IPEA/409).
12. ☒ A copy of the International Search Report (PCT/ISA/210).

Items 13 to 20 below concern document(s) or information included:

13. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
14. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
15. ☒ A **FIRST** preliminary amendment.
16. ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
17. ☐ A substitute specification.
18. ☐ A change of power of attorney and/or address letter.
19. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.
20. ☐ A second copy of the published international application under 35 U.S.C. 154(d)(4).
21. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
22. ☐ Certificate of Mailing by Express Mail
23. ☒ Other items or information:

Notice for Consideration of Documents Cited in International Search Report/Notice of Priority/Drawings (1 sheet)

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
09/926067	PCT/DE00/00276	211329US2PCT

24. The following fees are submitted:.	CALCULATIONS PTO USE ONLY
BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :	
☐ Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO **$1000.00**	
☒ International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO **$860.00**	
☐ International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO **$710.00**	
☐ International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) **$690.00**	
☐ International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) **$100.00**	
ENTER APPROPRIATE BASIC FEE AMOUNT =	**$860.00**
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (e)).	**$0.00**

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	
Total claims	8 - 20 =	0	x $18.00	**$0.00**
Independent claims	1 - 3 =	0	x $80.00	**$0.00**
Multiple Dependent Claims **(check if applicable)**.			☐	**$0.00**
TOTAL OF ABOVE CALCULATIONS			=	**$860.00**
☐ Applicant claims small entity status. (See 37 CFR 1.27). The fees indicated above are reduced by 1/2.				**$0.00**
SUBTOTAL			=	**$860.00**
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (f)).			+	**$0.00**
TOTAL NATIONAL FEE			=	**$860.00**
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) **(check if applicable).**			☐	**$0.00**
TOTAL FEES ENCLOSED			=	**$860.00**
			Amount to be: refunded	$
			charged	$

a. ☒ A check in the amount of **$860.00** to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. _____ in the amount of _____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. **15-0030** A duplicate copy of this sheet is enclosed.

d. ☐ Fees are to be charged to a credit card. **WARNING:** Information on this form may become public. **Credit card information should not be included on this form.** Provide credit card information and authorization on PTO-2038.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

Surinder Sachar
Registration No. 34,423

22850

Surinder Sachar
SIGNATURE

Marvin J. Spivak
NAME

24,913
REGISTRATION NUMBER

Aug. 23 2001
DATE

211329US

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF :

ANNIE STOESS ET AL : ATTN: APPLICATION DIVISION

SERIAL NO: NEW U.S. PCT APPLN :
(Based on PCT/DE00/00276)

FILED: HEREWITH :

FOR: OPTIMIZED BUS CONNECTION :
FOR MANAGING BUS
TRANSACTIONS

PRELIMINARY AMENDMENT

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

Prior to a first examination on the merits, please amend the above-identified application as follows:

IN THE SPECIFICATION

Please replace the title on page 1, line 1 with the following:

---OPTIMISED BUS CONNECTION FOR MANAGING BUS TRANSACTIONS---

IN THE CLAIMS

Please cancel Claims 1-4 without prejudice.

Please add new Claims 5-12 as follows:

5. (New) An optimized bus connection for acceptance of bus transactions, provided with a first store operating according to a FIFO principle, in which transaction processes

arriving from a processor system present at a higher level for execution by the optimized bus connection are temporarily stored in a sequence of the arriving transaction processes,

wherein,

following the first store, there is provided a first functional section for reading out, classifying, and typifying the bus transactions temporarily stored in the first store,

by means of the first functional section, those transactions that must be executed in a strictly logical sequence can be grouped respectively as a first class of transactions,

those transactions that do not have to be executed in a strictly logical sequence can be grouped respectively as a second class of transactions,

following the first functional section, there is provided a second functional section with a plurality of functional lines disposed in parallel, of which at least one functional line is allocated respectively to one of the two classes of transactions,

by means of the first functional section, depending on the result of its classification and typification of the transactions, the bus transactions can be allocated to one of the functional lines of the second functional section.

a first functional line allocated to the first class of transactions is provided with a storage structure functioning according to the FIFO principle,

a further functional line has a storage structure suitable for random accesses, and

following the second functional section, there is provided a third functional section with an execution unit common to the functional lines of the second functional section, by means of which the transactions contained in the individual functional lines of the second functional section can be organized into a serial sequence for forwarding to the processor system present at a higher level, and

the execution unit is configured to move a transaction of the second class ahead of a transaction of the first class, depending on a state of the higher-level processor system.

6. (New) An optimized bus connection according to Claim 5, wherein,

for the second class of transactions, there is provided in the second functional section on a basis of division of transactions into two types, which are read and write transactions, an independent functional line for each.

7. (New) An optimized bus connection according to Claim 5, wherein,

for bus transactions starting from the bus connection up to the execution unit of the third functional section, there is implemented a shortcut which operates on condition that an empty state exists in the first two functional sections.

8. (New) An optimized bus connection according to Claim 6, wherein,

for bus transactions starting from the bus connection up to the execution unit of the third functional section, there is implemented a shortcut which operates on condition that an empty state exists in the first two functional sections.

9. (New) An optimized bus connection according to Claim 5, wherein,

for the first class of transactions, starting from a point of arrival in the second functional section up to the execution unit of the third functional section, there is implemented a shortcut which operates on condition that an empty state exists in the functional line allocated to the first class.

10. (New) An optimized bus connection according to Claim 6, wherein,

for the first class of transactions, starting from a point of arrival in the second functional section up to the execution unit of the third functional section, there is implemented a shortcut which operates on condition that an empty state exists in the functional line allocated to the first class.

11. (New) An optimized bus connection according to Claim 7, wherein,

for the first class of transactions, starting from a point of arrival in the second functional section up to the execution unit of the third functional section, there is implemented a shortcut which operates on condition that an empty state exists in the functional line allocated to the first class.

12. (New) An optimized bus connection according to Claim 8, wherein,

for the first class of transactions, starting from a point of arrival in the second functional section up to the execution unit of the third functional section, there is implemented a shortcut which operates on condition that an empty state exists in the functional line allocated to the first class.

REMARKS

Favorable consideration of this application, as presently amended, is respectfully requested.

The present preliminary amendment is submitted to present new Claims 5-12 for examination. New Claims 5-12 are deemed to be self-evident from the original disclosure, including original Claims 1-4, and thus are not deemed to raise any issues of new matter.

The present application is believed to be in condition for a full and thorough examination on the merits. An early and favorable consideration of the present application is hereby respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Gregory J. Maier
Attorney of Record
Registration No. 25,599
Surinder Sachar
Registration No. 34,423

22850

(703) 413-3000
Fax No.: (703)413-2220
GJM/SNS:kst

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211329US

Marked-Up Copy
Serial No:

Amendment Filed on: 8/23/01

IN THE SPECIFICATION

Please replace the title on page 1, with the following:

[OLD TITLE] NEW TITLE

IN THE CLAIMS

Claims 1-4 (Cancelled).

Claims 5-12 (New).

Specification

Optimized bus connection for acceptance of bus transactions

The invention relates to an optimized bus connection for acceptance of bus transactions according to the preamble of claim 1.

The most diverse bus transactions take place in a processor system. Such bus transactions can be classified as those transactions which must be executed in a strictly logical sequence, and can be classified as those transactions which do not have to be executed in a strictly logical sequence.

Bus connections provided with a temporary store operating according to the FIFO principle are known for acceptance of bus transactions. In the temporary store operating according to the FIFO principle, bus transactions are temporarily stored in the sequence of their arrival in the sequence of their arrival and subsequently read out and executed in corresponding sequence, regardless of whether they must be or do not have to be executed in strictly logical sequence.

During bus transactions, it is frequently necessary to wait for results of other bus transactions, for example in order to be able to operate further with updated parameters. Because of the circumstance that the bus transactions are executed in the sequence of arrival, bus transactions which are independent of such transactions must nevertheless wait until the transactions that arrived earlier have been completed. The overall result is slowing and thus loss of performance of the processor system.

The object of the present invention is to provide an optimized bus connection, by which the working speed of a processor

system is accelerated and thus its performance capability is increased.

Starting from a bus connection of the type cited in the introduction, this object is achieved by an optimized bus connection which is provided with the features of claim 1.

Such a bus connection classifies and typifies the arriving bus transactions and allocates them to respective functional lines disposed in parallel. Depending on the class or type of a transaction, the transactions are temporarily stored in the various functional lines in such a way that, on the one hand, they can be treated according to their class or type and, on the other hand, they are sufficiently separated from one another that an adapted sequence can be selected in the sequence of execution. Contributing to this is the fact that some functional lines have a parallel structure. Thus transactions can be moved to the front with the inventive bus connection, so that waiting times until completion of a previously arrived transaction can be eliminated in many cases. The result is acceleration of the mode of operation and thus increased performance capability of a processor system.

Advantageous embodiments of the invention are subject matter of dependent claims.

Accordingly, not only are transactions pending for execution separated according to whether or not they must be executed according to a strictly logical sequence, but also the transactions that do not have to be executed strictly according to a logical sequence are further separated according to whether they are transactions of the read or write type. Read transactions in particular are determining for the performance of an overall system. They must therefore

be given special priority in execution.

As explained in the foregoing, the inventive bus connection eliminates congestion effects which can occur among transactions pending for execution. In the absence of congestion effects, it is possible that entire functional lines will remain almost empty, because arriving transactions can be executed immediately. In order to save further on time needed to transport transactions through the so-called empty functional lines, advantageous embodiments of the invention are provided with shortcuts which bypass the so-called empty functional lines.

A practical example of the invention will be explained in more detail hereinafter with reference to a drawing. Therein the single figure shows an optimized bus connection according to the invention.

The figure shows a processor bus PB, which is part of a higher-level processor system, not indicated in more detail in the figure.

To processor bus PB there is connected a first temporary store S1, which is known in itself and operates according to the FIFO principle, and which stores the arriving bus transactions in their sequence of arrival.

Following first store S1, there are provided three functional sections I, II and III connected in series, of which first functional section I is responsible for reading out, classifying and typifying, by means of a decoder DK, as fast as possible, the transactions temporarily stored in first store S1. On the basis of the classification, the transactions are classified into those transactions that must be executed

in strictly logical sequence. In addition, the transactions are classified into those transactions that do not have to be executed in strictly logical manner. Within the group of transactions that do not have to be executed in strictly logical sequence, a deeper-level typification is performed as to whether the transactions are transactions of the read type or write type.

Second functional section II receives, according to typification and classification, in one of three further stores S2, S3, S4, each of which is disposed in its own allocated functional line, the transaction processes typified and classified by decoder DK.

The transactions classified in the "execution in strictly logical sequence" class are received in store S2 regardless of whether they correspond to the "write" or "read" type. Since these transaction processes must be executed in strictly logical sequence, a deeper-level subdivision into such types is not useful.

Transactions which correspond to the "write" type have allocated to a first write store SS1, in which the information bits to be written can be received. If an individual processor connected to processor bus PB starts a transaction process of the "execution in strictly logical sequence" class and of the "write" type, it transfers the corresponding transaction process together with the information bits to be written to first functional section I. In this way the transaction process for the individual processor is ended. It can be devoted to other tasks. First functional section I ensures that the transaction process is written into second store S2 and the information bits to be written are written into first write store SS1, each of second functional section II. Second

store S2 is designed according to the FIFO principle, in order to be able thereby to maintain the strictly logical sequence of execution of the transaction processes.

In the present practical example, transaction processes of the "execution not in strictly logical sequence" class and of the "read" type are stored in store S3 of second functional section II. Since the sequence of execution is unrestricted, store S3 is designed according to a parallel structure, from which contents can be extracted optionally. The same is true for store 4 of second functional section II, only in regard to the "write" type with the "execution not in strictly logical sequence" transaction class. Since store S4 is responsible for transaction processes of the "write" type, a second write store SS2 is allocated to this store in a manner corresponding to first write store SS1.

Stores S3 and S4 ensure that, in particular, the transactions of the "execution not in strictly logical sequence" class and of the "read" type can be executed immediately and the transaction processes of the "execution not in strictly logical sequence" class of the "write" type can be executed as soon as possible.

The components of second functional section II allocated to respective functional lines lead to an execution unit AE which is common to the functional lines of second functional section II and which is disposed in third functional section III. With the transactions obtained from the functional lines of second functional section II, execution unit AE provides for serial sequencing for further processing, while taking into consideration the importance of the origin of the transactions from the functional lines. In this way, transactions of the "execution not in strictly logical sequence" class may be

moved ahead of transactions of the "execution in strictly logical sequence" class. The transactions rearranged in more favorable sequence in this way are then forwarded to a system bus SB, which is also part of the higher-level processor system not indicated in more detail in the figure.

Shortcuts KW1 and KW2 permit the transaction processes to jump over individual functional sections. For example, if the successive components of functional sections I and II are empty, a transaction process can travel directly from processor bus PB via shortcut KW1 into execution unit AE of functional section III. If store S2 operating according to the FIFO principle in functional section II is empty, an arriving transaction process can be transferred immediately through the store and directed to execution unit AE of functional section III. In both cases, time is saved for transaction processes which affect through transport.

Claims

1. An optimized bus connection for acceptance of bus transactions, provided with a first store S1 operating according to the FIFO principle, in which transaction processes arriving from a processor system present at a higher level for execution by the optimized bus connection are temporarily stored in the sequence of the arriving transaction processes, characterized in that, following the first store (S1), there is provided a first functional section (I), by which the bus transactions temporarily stored in the first store S1 are read out, classified and typified as fast as possible, in that, following the first functional section, there is provided a second functional section (II) with a plurality of functional lines disposed in parallel, of which at least one is allocated respectively to one class of transactions, in that, by means of the first functional section (I), those transactions that must be executed in a strictly logical sequence are grouped respectively as one class of transactions on the one hand and those transactions that do not have to be executed in a strictly logical sequence are grouped respectively as one class of transactions on the other hand, in that, by means of the first functional section (I), depending on the result of its classification and typification of the transactions, the bus transactions are allocated to one of the functional lines of the second functional section (II), in that the functional line allocated to the class of transactions that must be executed in strictly logical sequence is provided with a storage structure functioning according to the FIFO principle, in that the other functional lines have a storage structure suitable for random accesses, and in that, following the second functional section (II), there is provided a third functional section (III) with an execution unit (AE) common to the functional lines of the

second functional section (II), by means of which the transactions contained in the individual functional lines of the second functional section (II) are organized into a serial sequence for forwarding to the processor system present at a higher level, with the feature that, in given cases, depending on the requirements on the higher-level processor system, transactions from the class of transactions that do not have to be executed in strictly logical sequence are moved ahead of the transactions of the class of transactions that must be executed in strictly logical sequence.

2. An optimized bus connection according to claim 1, characterized in that, for the class of transactions that do not have to be executed in strictly logical sequence, there is provided in the second functional section (II), on the basis of division of transactions into two types, which are read and write transactions, an independent functional line for each.

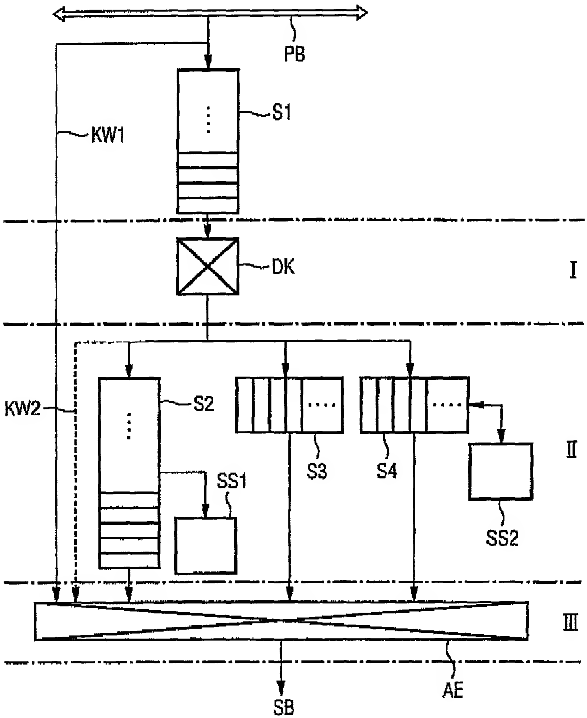
3. An optimized bus connection according to claim 1 or 2, characterized in that, for bus transactions starting from the bus connection up to the execution unit (AE) of the third functional section (III), there is implemented a shortcut (KW2) which operates on condition that an empty state exists in the first two functional sections (I, II).

4. An optimized bus connection according to one of the preceding claims, characterized in that, for the class of transactions that must be executed in strictly logical sequence, starting from a point of arrival in the second functional section (II) up to the execution unit (AE) of the third functional section (III), there is implemented a shortcut (KW2) which operates on condition that an empty state exists in the functional line allocated to that class.

Abstract

Optimized bus connection for acceptance of bus transactions

For optimization of the mode of operation of processor systems, there is proposed a bus connection which divides bus transactions substantially into transactions that must be executed in strictly logical sequence and that do not have to be executed in strictly logical sequence. Subsequently the transactions are again arrayed one after another in serial manner for further processing, with the feature that, in given cases, transactions that do not have to be executed in strictly logical sequence are moved ahead of transactions that must be executed in strictly logical sequence. The result is a gain in time and thus performance for the processor system.


PB
S1
KW1
DK
I
KW2
S2
SS1
S3
S4
SS2
II
III
SB
AE

Declaration and Power of Attorney for Patent Application
Erklärung für Patentanmeldungen mit Vollmacht
German Language Declaration

Als nachstehend benannter Erfinder erkläre ich hiermit an Eides Statt:

As a below named inventor, I hereby declare that:

daß mein Wohnsitz, meine Postanschrift und meine Staatsangehörigkeit den im nachstehenden nach meinem Namen aufgeführten Angaben entsprechen, daß ich nach bestem Wissen der ursprüngliche, erste und alleinige Erfinder (falls nachstehend nur ein Name angegeben ist) oder ein ursprünglicher, erster und Miterfinder (falls nachstehend mehrere Namen aufgeführt sind) des Gegenstandes bin, für den dieser Antrag gestellt wird und für den ein Patent für die Erfindung mit folgendem Titel beantragt wird:

My residence, post office address and citizenship are as stated next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

OPTIMISED BUS CONNECTION FOR MANAGING BUS TRANSACTIONS

deren Beschreibung:

- ☐ ist beigefügt
- ☐ wurde angemeldet am _____

unter der US-Anmeldenummer oder unter der internationalen Anmeldenummer im Rahmen des Vertratgs über die Zusammenarbeit auf dem Gebiet des Patentwesens (PCT)

_____ und am

_____ abgeändert (falls zutreffend).

the specification of which:

- ☐ is attached hereto.
- ☐ was filed on PCT/DE00/00276

as United States Application Number or PCT International Application Number

1 February 2000 and was amended on

_____ (if applicable).

Ich bestätige hiermit, daß ich den Inhalt der oben angegebenen Patentanmeldung, einschließlich der Ansprüche, die eventuell durch einen oben erwähnten Zusatzantrag abgeändert wurde, durchgesehen und verstanden habe.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

Ich erkenne meine Pflicht zur Offenbarung jeglicher Informationen an, die zur Prüfung der Patentfähigkeit in Einklang mit Titel 37, Code of Federal Regulations, § 1.56 von Belang sind.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

German Language Declaration

Ich beanspruche hiermit ausländische Prioritätsvorteile gemäß Title 35, US-Code, § 119(a)-(d), bzw. § 365(b) aller unten aufgeführten Auslandsanmeldungen für Patente oder Erfinderurkunden, oder § 365(a) aller PCT internationalen Anmeldungen, welche wenigstens ein Land ausser den Vereinigten Staaten von Amerika benennen, und habe nachstehend durch ankreuzen sämtliche Auslandsanmeldungen für Patente bzw. Erfinderurkunden oder PCT internationale Anmeldungen angegeben, deren Anmeldetag dem der Anmeldung, für welche Priorität beansprucht wird, vorangeht.

I hereby claim foreign priority under Title 35, United States Code, § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT International application which designated at least one country other than the United States, listed below, and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior foreign application(s) (Frühere ausländische Anmeldungen)			Priority claimed Priorität beansprucht	
199 08 414.9	GERMANY	26 February 1999	☒ Yes Ja	☐ No Nein
(Number) (Nummer)	(Country) (Land)	(Day/Month/Year Filed) (Tag/Monat/Jahr der Anmeldung)		
			☐ Yes Ja	☐ No Nein
(Number) (Nummer)	(Country) (Land)	(Day/Month/Year Filed) (Tag/Monat/Jahr der Anmeldung)		

Ich Beanspruche hiermit Prioritätsvorteile unter Title 35, US-Code, § 119(e) aller US-Hilfsanmeldungen wie unten aufgezählt.

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below

(Application No.) (Aktenzeichen)	(Filing Date) (Anmeldetag)	(Application No.) (Aktenzeichen)	(Filing Date) (Anmeldetag)

Ich beanspruche hiermit die mir unter Title 35, US-Code, § 120 zustehenden Vorteile aller unten aufgeführten US-Patentanmeldungen bzw. § 365(c) aller PCT internationalen Anmeldungen, welche die Vereinigten Staaten von Amerika benennen, und erkenne, insofern der Gegenstand eines jeden früheren Anspruchs dieser Patentanmeldung nicht in einer US-Patentanmeldung, bzw. PCT internationalen Anmeldung in in einer gemäß dem ersten Absatz von Title 35, US-Code, § 112 vorgeschriebenen Art und Weise offenbart wurde, meine Pflicht zur Offenbarung jeglicher Informationen an die zur Prüfung der Patentfähigkeit in Einklang mit Title 37, Code of Federal Regulations, § 1.56 von Belang sind und die im Zeitraum zwischen dem Anmeldetag der früheren Patentanmeldung und dem nationalen oder im Rahmen des Vertrags über die Zusammenarbeit auf dem Gebiet des Patentwesen (PCT) gültigen internationalen Anmeldetags bekannt geworden sind.

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s), or § 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application.

(Application No.) (Aktenzeichen)	(Filing Date) (Anmeldetag)	(Status) (patented, pending, abandoned) (Status) (patentiert, schwebend, aufgegeben)
PCT/DE00/00276	1 February 2000	
(Application No.) (Aktenzeichen)	(Filing Date) (Anmeldetag)	(Status) (patented, pending, abandoned) (Status) (patentiert, schwebend, aufgegeben)

Ich erkläre hiermit, daß alle in der vorliegenden Erklärung von mir gemachten Angaben nach bestem Wissen und Gewissen der Wahrheit entsprechen, und ferner daß ich diese eidesstattliche Erklärung in Kenntnis dessen ablege, daß wissentlich und vorsätzlich falsche Angaben oder dergleichen gemäß § 1001, Title 18 des US-Code strafbar sind und mit Geldstrafe und/oder Gefängnis bestraft werden können und daß derartige wissentlich und vorsätzlich falsche Angaben die Rechtswirksamkeit der vorliegenden Patentanmeldung oder eines aufgrund deren erteilten Patentes gefahrden können.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

German Language Declaration

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POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith *(list name and registration number)*

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(703) 413-3000

Vor- und Zuname des einzigen oder ersten Erfinders	Full name of sole or first inventor Annie STOESS
Unterschrift des Erfinders Datum	Inventor's signature Date Annie Stoess 09. August 2001
Wohnsitz	Residence Adlfurt 8, D-83043 Bad Aibling Germany
Staatsangehörigkeit	Citizenship France
Postanschrift	Post Office Address same as above

Vor- und Zuname des zweiten Miterfinders (falls zutreffend)	Full name of second joint inventor, if any Johann SCHACHNER
Unterschrift des zweiten Erfinders Datum	Second inventor's signature Date Johann Schachner 09. August 2001
Wohnsitz	Residence Oedenstockacherstrasse 1, D-85640 Putzbrunn, Germany
Staatsangehörigkeit	Citizenship Germany
Postanschrift	Post Office Address same as above

(Im Falle dritter und weiterer Miterfinder sind die entsprechenden Informationen und Unterschriften hinzuzufugen.)

(Supply similar information and signature for third and subsequent joint inventors.)

German Language Declaration

Vor- und Zuname des dritten Miterfinders (falls Zutreffend)	Full name of third joint inventor, if any Wolfgang ZIEMANN
Unterschrift des dritten Erfinders Datum	Third inventor's signature Date 09. August 2001
Wohnsitz	Residence Tulpenweg 3, D-85635 Hoehenkirchen-Siegertsbrunn, Germany
Staatsangehörigkeit	Citizenship Germany
Postanschrift	Post Office Address same as above
Vor- und Zuname des vierten Miterfinders (falls Zutreffend)	Full name of fourth joint inventor, if any
Unterschrift des vierten Erfinders Datum	Fourth inventor's signature Date
Wohnsitz	Residence
Staatsangehörigkeit	Citizenship
Postanschrift	Post Office Address
Vor- und Zuname des fünften Miterfinders (falls Zutreffend)	Full name of fifth joint inventor, if any
Unterschrift des fünften Erfinders Datum	Fifth inventor's signature Date
Wohnsitz	Residence
Staatsangehörigkeit	Citizenship
Postanschrift	Post Office Address
Vor- und Zuname des sechsten Miterfinders (falls Zutreffend)	Full name of sixth joint inventor, if any
Unterschrift des sechsten Erfinders Datum	Sixth inventor's signature Date
Wohnsitz	Residence
Staatsangehörigkeit	Citizenship
Postanschrift	Post Office Address

(Im Falle dritter und weiterer Miterfinder sind die entsprechenden Informationen und Unterschriften hinzuzufügen.)

(Supply similar information and signature for third and subsequent joint inventors.)